REMARKS

Claims 1-2, 6, 10, 11, and 21-22 remain pending in the application with the present amendments. The claims are amended herein in the manner recommended by the examiner to address the objections thereto under 35 U.S.C. §112.

Applicants thank the examiner for the courtesy extended in granting the telephonic interview conducted on March 25, 2008. During the interview, amendatory language was discussed to address the rejections under 35 U.S.C. §112. In addition, the language of the claims was discussed in relation to the teachings of the art cited in the final office action. No agreement was reached to allow claims at this time. Reconsideration and withdrawal of the rejections is respectfully requested in view of the present amendments.

In the Office Action, claims 1, 2, 6, 11 and 21 were rejected under 35 U.S.C. §103(a) over U.S. Patent No. 5,369,642 to Shioka et al. ("Shioka") in view of U.S. Patent Pub. No. 2003/0054592 to Farnworth et al. ("Farnworth"). For the reasons set forth below, applicants respectfully submit that the claims overcome the rejections over the references cited in the final Office Action.

As amended herein, claim 1 recites an apparatus including an "integrated circuit" in which an individual integrated circuit has a plurality of data transmitters including a plurality of default data transmitters, at least one redundancy data transmitter and a plurality of connection elements each used to conductively connect or disconnect the default data transmitter and conductively connect or disconnect the redundancy data transmitter. Applicants have given the term "integrated circuit" its ordinary meaning, i.e., a

"chip" (applicants' specification at paragraphs [0002]-[0003]). Support for the recitation that the data transmitters and connection elements are incorporated in an individual integrated circuit is provided at paragraph [0011] and [0019]. Paragraph [0019] describes an embodiment in which an individual integrated circuit having multiple data transmitters described in the background section of applicants' specification at paragraphs [0005] and [0006] is augmented with modifiable connection elements on the chip.

Shioka describes a switcher 200 for a signal transmission system (FIG. 3) which includes relay switches (col. 6, lns. 59-61) for making and breaking circuit connections between signal lines and regular transmitters and doing the same with respect to a standby transmitter. Shioka describes a system in which data transmitters output signals onto a balanced two-core cable (col. 4, lns. 31-32; col. 3, ln. 32) or coaxial cables (col. 4, lns. 37-38). Switches are connected between the connectors (e.g., coaxial connectors (col. 4, lns. 39-40)) of these cables at locations between the transmitters. Balanced two-core cables and coaxial cables described in Shioka are not found incorporated within chips, but rather, only in much larger systems such as between boards of a switching system. At best, Shioka teaches a system in which data communication signals are switched between the outputs of data transmitters and output signal lines by switching devices, e.g., relays at an illustrative bit rate of 2048 bits per second (col. 1, ln. 36). Like the MOSFET-switching arrangement described in the background section of applicants' Specification, the switching devices described in Shioka are poorly suited to switching data communication signals from data transmitters onto output signal lines at

signal switching frequencies above about 500 MHz.

Farnworth teaches a wafer-level system in which fuses and antifuses of off-die logic circuits 30 provided in streets 31 between dies 12 (or "chips") of a wafer connect or disconnect circuit elements of a die 12 through a set of additional conductive paths 32 functioning as "discretionary wiring". (paragraphs [0016]-[0020]). All of the fuses and antifuses used to connect or disconnect circuit elements are not incorporated within the die 12 on which the primary circuit elements are located, but rather only in the off-die circuits 30. Farnworth makes no reference to using fuses or antifuses to connect data transmitters to output signal lines for transmitting data communication signals at signal switching frequencies over 500 MHz through such fuses or antifuses onto signal lines.

The combination of Shioka with Farnworth fails to teach an apparatus comprising an integrated circuit or chip in which an individual integrated circuit includes a fuse, an antifuse or both for conductively connecting and disconnecting a default data transmitter on the same chip to an output signal line for transmitting a data communication signal above about 500 megahertz through such fuse or antifuse onto the output signal line and for conductively disconnecting and connecting a redundancy data transmitter to the output signal line.

Providing fuse or antifuse switching elements on an individual integrated circuit between data transmitters and output signal lines for carrying such high frequency data communication signals yields a different type of system from that taught by the combination of Shioka and Farnworth. The combination of Shioka and Farnworth fails to

teach an apparatus as recited in claim 1 including an integrated circuit wherein an individual integrated circuit includes a fuse which connects a data transmitter to an output signal line for transmission of a data communication signal through the fuse onto the output signal line at a signal switching frequency above about 500 MHz.

Moreover, in the integrated circuit recited in claim 1, redundancy replacement of a faulty transmitter is self-contained on a chip. Integration of function on one integrated circuit reduces complexity. Because connection elements having fuses/antifuses are integrated on the chip rather than on off-chip devices, the integrated circuit recited in claim 1 eliminates the external conductive data paths 32 (discretionary wiring) of Farnworth or the analogous additional cables, coaxial connectors and external switches of Shioka.

Claim 21 has recitations similar to those of claim 1 and is believed to be patentable over the combination of Shioka and Farnworth for at least the same reasons as discussed above.

Claims 2, 6 and 11 depend from claim 1 and are believed to be fully distinguished from the combination of references for at least the same reasons as discussed above.

Claim 22 was rejected under 35 U.S.C. §103(a) over Shioka in view of U.S. Patent No. 6,819,197 to Maldanado ("Maldanado"). Similar to that discussed above, Shioka fails to teach *an integrated circuit* or chip having a plurality of default data transmitters, a redundancy data transmitter and a plurality of first and second connection elements used to connect or disconnect a first default data transmitter to corresponding

input and output signal lines. Maldanado fails to provide the teachings which are lacking in Shioka. Maldanado fails to teach MEM switches incorporated in an integrated circuit or chip used to connect and disconnect a default data transmitter incorporated in the chip from corresponding input and output signal lines.

Claim 10, which depends from claim 22 is believed to be patentable for at least the same reasons as discussed with respect to claim 22.

In view of the present amendments and remarks, it is believed that the application is now in condition for allowance. If, for any reason, the examiner does not believe that such action can be taken at this time, it is requested that he telephone the undersigned at the number indicated below to discuss any issues that remain.

If any fees are required for which express authorization has not been provided, authorization is given to debit the Deposit Account No. 09-0458 of the Assignee International Business Machines Corporation. If there is an overpayment, please credit the same account.

Respectfully submitted,
Louis L. Hsu et al.

By: _____

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